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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,159	10/29/2003	Jurgen Amon	1406/177	7637

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,159	AMON ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 page*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Preliminary Amendment

1. Preliminary Amendment filed on 10/29/03 has been entered and made of record.

In Preliminary Amendment, claims 1-16 and specification have been amended.

Priority

2. Acknowledge is made of applicants' claim for foreign priority base on an application 10250872 filed in Germany on 10/31/2002.

Information Disclosure Statement

3. Information Disclosure Statement (IDS) filed on **11/21/03** and made of record. The references cited on the PTOL 1449 form have been considered.

Drawings

4. The drawings are objected to for the following reasons.

Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (specification, pages 2-3). See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office

action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1 is rejected under 35 USC 102 (e) as being anticipated by applicant submitted prior art (AAPA).

Regarding claim 1, AAPA discloses a method for forming a semiconductor structure similar to what recited in claim 1, see Fig. 3 and "Background Art" in Specification, pages 2-3, the method having a plurality of gate stacks GS1, GS2 on a semiconductor substrate 10, having the following steps: application of the gate stacks GS1, GS2 to a gate dielectric 11 above the substrate 10, formation of a sidewall oxide 17, 19 on sidewalls of the gate stacks, application and patterning of a mask 12A, 12B on a semiconductor structure, implantation of a contact doping 13 in a self-aligned manner with respect to the sidewall oxide 17, 19 of the gate stack regions not covered by the mask (See Fig. 3).

8. Claims 1-11, 13 are rejected under 35 USC 102 (e) as being anticipated by Divakaruni et al., U.S. Patent No. 6,444,548.

Regarding claim 1, Divakaruni et al. discloses a method for forming a semiconductor structure similar to what recited in claim 1, see Figs. 3-4, 5A-5C, 6A-6C, and Cols. 1-10, the method having a plurality of gate stacks (fig. 3) on a semiconductor substrate, having the following steps: application of the gate stacks GC to a gate dielectric above the substrate, formation of a sidewall oxide 305 on sidewalls of the gate stacks, application and patterning of a mask BPSG, PR on a semiconductor structure, implantation of a contact doping CB 306 in a self-aligned manner with respect to the

sidewall oxide of the gate stack regions not covered by the mask (See Figs. 3 and 5A and Cols. 3-4).

Regarding claim 2, it is inherent that the sidewall oxide is reduced in its lateral extent in regions not covered by the mask after the implantation of the contact doping occurs. Regarding claim 3, Divakaruni et al. discloses wherein the reduction of the extend of the lateral sidewall oxide is followed by a further implantation of different doping (Fig. 6A).

Regarding claim 4, Divakaruni et al. discloses the further doping (halo doping) is a p-type (boron) having a low concentration (Cols. 4-6) preferably at least a power of ten lower than the contact doping concentration.

Regarding claim 5, Divakaruni et al. discloses wherein the further doping is a bit line halo doping implanted from a predetermined direction at an angle preferably in the range of between 0 to 30 o inclusive (Fig. 6A, lines 35-65, Col. 5).

Regarding claim 6, Divakaruni et al. discloses wherein the contact doping 306 is implanted at a angle of 0^{o} (Fig. 5A).

Regarding claim 7, Divakaruni et al. discloses wherein the contact doping is an n-type doping with arsenic (lines 30-40, Col. 4; line s10-20, Col. 5).

Regarding claim 8, Divakaruni et al. discloses wherein a removal of the mask is followed by an implantation of, example, dopant having a lower dopant concentration than that of the contact doping (lines 45-55, Col. 5).

Regarding claims 9-11, Divakaruni et al. discloses wherein the gate stacks are applied approximately with respect to one another and the method is used to form logic transistors, selection transistors, DRAM (Figs. 5A-5C, 6A-6C; Cols. 1-2, 4-6).

Regarding claim 13, Divakaruni et al. discloses the gate stacks are provided paralled and in strip-type fashion on the substrate (Figs. 3-6).

9. Claims 12, 14-16 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Divakaruni et al., U.S. Patent No. 6,444,548.

Regarding claim 12, Divakaruni et al. discloses the formation of gate stack but fails to disclose the length of gate stack is less than 200 nm, however, the selection of such parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, or in conbination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See*

also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Regarding claim 14, Divakaruni et al. discloses the gate stack is formed of conductive material and cap layer nitride. It would have been well known in the art that the conductive material for gate stack would have been polysilicon and an overlying second layer made of a metal silicide or a metal since the polysilicon is well known to be used as gate conductive material and the overlying second layer of silicide or metal is well known to be used to reduce resistance of gate stacks.

Regarding claims 15-16, Divakaruni et al. discloses the layer above the gate stack is silicon nitride (NIT, Fig. 3).

10. The other references cited in PTO-892 also disclose the present invention as cited in claim 1.

11. When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le
Examiner
Art Unit 2818